

## REMARKS

Claims 1-7, 10-18, 21-29, 32-33, 37-41, and 43-50 stand rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Pat. to Wollan et al.<sup>1</sup> ("Wollan"). In addition, claims 1-7, 10-18, 21-29, 32-33, 37-41, stand rejected under 35 U.S.C. §103(a) as being obvious in view of Wollan. Moreover, claims 1-7, 10-18, 21-29, 32-33, 37-42 stand rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Pat. to Potter, et al.<sup>2</sup> ("Potter").

Claims 1-3, 12-13, 23-25, and 37-38 have been amended. Claims 4-11, 14-22, 26-36, and 39-50 have been cancelled. Applicant respectfully traverses the rejections.

A. One "advantage of the invention is that a CPU 22, using an N-bit data bus 26 addressing a memory device 51, 56, 60 having a  $2^M$  bit memory space where M is greater than N, consumes fewer "cycles" than was formerly required."<sup>3</sup> Amended claims 1 and 23 are directed to accessing a memory using indirect addressing using fewer bus cycles than required in the prior art. In contrast, a known indirect addressing technique disclosed in the present application required twice as many bus cycles as that claimed. Wollan fails to disclose or suggest an indirect addressing method that uses fewer bus cycles than required in the prior art. Potter discloses using separate buses for address and data, and therefore does not disclose a number of bus cycles required when using a single bus for both address and data.

B. In rejecting previously presented claims 12 and 37, the Office Action does not point to a particular part disclosed in the Wollan reference that counts address-bytes received on the bus. Rather, according to the Office Action, the claimed address-byte-received counter is taught "as the system keeping track of the first half of the 16 bit logical address otherwise the system would not place the second half of the 16 bit logical address in the correct register." It is certainly true that if the Wollan microcontroller is operable, it must have some way of keeping track of first and second halves of a 16-bit logical address. However, Wollan does not disclose how it keeps track of first and second address halves. According to the Office Action, this does not present a problem because to require the reference to

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<sup>1</sup> No. 5,809,327

<sup>2</sup> No. 5,170,477

<sup>3</sup> Present application, para. [0044].

explicitly disclose that it uses a counter to keep track first and second address halves is similar to demanding that a reference which discloses a memory element state that the memory element is comprised of silicon, buses, or transistors.

According to the Office Action, a counter is a "common, necessary piece found in all addressing structures."

First, to say that a reference which discloses a memory element also discloses that the memory element is comprised of silicon, buses, or transistors is equivalent to saying that the reference *inherently* discloses the material or parts. Applicant understands that the Examiner has the burden of proof when relying on a reference for claim element asserted to be inherently disclosed. "In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art."<sup>4</sup>

Moreover, "to establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.' "<sup>5</sup> The Office Action says that "in order for the system to utilize the pairs of 16 bit registers, the first byte *is* counted as the first half of the total of 16 bits address."<sup>6</sup> However, there is no disclosure that anything is counted. An alternative to this possibility is found in the background of the present application. Wollan discloses that each of the registers found in the register file 20 have an address.<sup>7</sup> The indirect addressing technique disclosed in the background of the present application provides for transmitting a first address to identify a first register and then transmitting a second address to identify a second register. It is possible the Wollan uses the pair of 16 bit registers by retrieving register addresses for lower and upper bytes from a memory and then placing the lower and upper byte addresses on the eight-bit bus in respective address cycles.

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<sup>4</sup> MPEP 2112 IV., citing *Ex parte Levy*, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original).

<sup>5</sup> MPEP 2112 IV., citing *In re Robertson*. See also Ex Parte Mary Smith, BAPI 2007-1925 (2007).

<sup>6</sup> Emphasis added.

<sup>7</sup> See last paragraph of Wollan claim 1.

C. Accordingly, neither the Wollan nor the Potter references discloses each and every element of independent claims 1, 12, 23, and 37. Claims 2-3, 13, 24-25, and 38 depend from one of the independent claims. Accordingly, these dependent claims are not anticipated for at least the same reasons that the independent claims are not anticipated.

D. With respect to the rejections under 35 U.S.C. §103(a), the Office Action does not identify a reason why a person of ordinary skill in the art would have combined prior elements in the manner claimed. Therefore, the Office Action does not establish a *prima facie* case of obviousness.

Conclusion

Accordingly, claims 1-3, 12-13, 23-25, and 37-38 are in condition for allowance. Applicant respectfully requests that claims 1-3, 12, 23-25, and 37 be allowed, and this application be passed to issue. Should the Examiner feel that a telephone conference would expedite prosecution of this application, the Examiner is invited to call Applicant's attorney, Richard A. Wilhelm (48,786), at (503) 635-1187.

Respectfully submitted,

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